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Control Design, Analysis and Comparative study of Different Control Strategies of a Bidirectional DC/DC Multiport Converter for Electric Vehicles

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Executive Summary

Multiport converters (MPCs) represent a valuable solution when multiple sources are present in an electric vehicle. The control strategies of these MPCs are one of the key elements that may have a significant impact on the vehicle performances. The interleaving technique enhances the performances of the DC/DC converters by paralleling and shifting the commutation instances of the parallel phases. In addition, as multiple ports are present, these are also interleaved arising the concept of port interleaving. Here a mix of control strategies is used to take advantage of the MPC. State-feedback control at the voltage port and feedback linearization at the current port shows superior results in simulation when compared with other standard techniques.

1 Introduction

An electric vehicle (EV) can combine multiple sources in its powertrain to exploit the advantages of each source. Several cases can be found in literature where different arrangements of Fuel Cells (FC), batteries and ultracapacitors (UC) were used to drive an EV [1]–[7]. However, each source has its own voltage range of operation, which imposes a power electronics interface to integrate various sources with the load.

More specifically, batteries and ultracapacitors face a voltage drop during operation and they require a DC/DC converter to regulate the voltage to the required level.

Nowadays, Lithium nickel manganese cobalt oxide (NMC) batteries are dominating the Battery Electric Vehicle (BEV) market given their stronger power/energy performance when compared to other technologies [8]. Despite having a higher operating voltage when compared to lithium iron phosphate (LFP) batteries, the NMC batteries have a wider voltage window of operation resulting in a 20 % of voltage drop from full charge to 10 % State of Charge (SoC). In addition, a Low Voltage (LV) battery bank suffers less of imbalances compared with a High Voltage (HV) battery bank [9], [10] and is able to recover more energy from regenerative braking. On the other hand, in an EV, during a drive cycle the batteries suffer from frequent charge and discharge at high current rate that affect the battery lifetime [9]. Therefore, a hybrid configuration including an UC bank could achieve better performances as the UC bank can handle

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the power flow during the high dynamic behavior of the vehicle. However, to make a reasonable usage of the UC bank (75 %), the UC voltage swings between its full voltage and half voltage. As a result, the UC bank is often used together with a DC/DC converter that regulates its output voltage.

As it is clear, each source can be combined with a power electronics converter to enhance its capabilities. Unfortunately, each converter adds extra losses and weight to the system that might jeopardize the convenience of having multiple sources in the drivetrain. The idea to combine multiple converters into a single component arose the concept of Multiport Converters (MPC). The MPC idea has been synthesized into several topologies, all aimed to share the components of the multiple converters as inductors, switches and capacitors[1], [4], [11]–[14]. Among all the topologies presented, the authors decided for this study to focus on the topology presented in [1] with the modification of the interleaving technique applied to each port, as shown in Figure 1 -1. The reason has to be addressed to the advantage of controlling the ports separately and with bidirectional capabilities each. Moreover, the topology in [1] is suitable for applying the interleaving concept to both the phases and the ports.

The interleaving concept in power electronics found its first applications in the area of aerospace [15] thanks to its capability to reduce the ripple amplitude and increase in ripple frequency. Since then, interleaving techniques were applied in domains where stringent requirements on input current ripple and weight were needed. More specifically, in Fuel Cell Hybrid Vehicles (FCHV) a unidirectional interleaved boost converter (IBC) is used to reduce the input current ripple which is responsible for the lifetime decrease in a fuel cell stack [16]–[18]. In a similar way, in EVs, DC/DC converters are applied to boost the low voltage of the battery pack to the higher voltage of the electric motor. The interleaved technique can thus be applied to reduce the power density of the converter as in [19]. However, for some usual control strategies more phases mean more control variables to be measured and controlled increasing the complexity of the control system.

In [20] the Kboost approach has been presented as a simple way to synthesize a feedback amplifier to obtain the desired crossover frequency and phase margin. In [21] the Kboost approach is used to design a double lead-lag controller for voltage mode control. In [18], the linearized averaged small signal models for an interleaved converter are derived and a dual loop control with single lead-lag controller is designed. Furthermore, in [22] a state-feedback control is designed for interleaved converters.

In a similar way to the combination of sources, a MPC can exploit the advantages of each control strategy by applying them to different ports. In fact, one port is meant to control the power flow, while the other one regulates the output voltage. The source with the fastest dynamic response is responsible for the voltage regulation task such that to reject quickly the disturbances on the output voltage.

In this paper, both the interleaved and multiport concepts are used to synthesize an Interleaved Multi-Port bidirectional Converter (IMPC), as already presented in [4] and shown in Figure 1 -1. Port a is dedicated to the Ultra-Capacitor (UC) bank and has 3 phases interleaved due to a wider input voltage operation, while port b can be used for battery or Fuel Cell source where the input voltage can be considered constant.

Voltage-mode control, average current mode control, state feedback control and feedback linearization control are in this paper applied and mixed together to find the best combination of control strategies that increases the performances of the MPC for vehicle applications. The main source, battery pack or FC, requires having a slow dynamic to preserve its lifetime. Therefore, the current is forced to follow a defined slope during acceleration or deceleration. For sake of simplicity, the dynamics of the sources are scaled up. This means that the slew rate given to the battery current reference is not realistic, and it was scaled to keep the computation time low. However, it is able to give information to the performances of the controller.

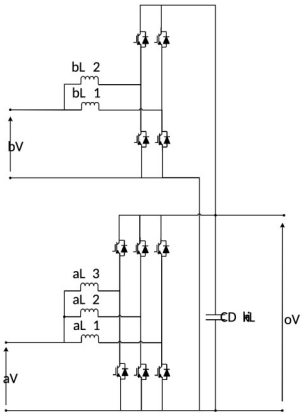


Figure 1-1 Interleaved Multiport Bidirectional Converter

2 Interleaved Multiport DC/DC modelling techniques

The IMPC presents several phases (N) needed to realize the interleaving concept, but it has only one capacitor shared by the different ports (M). Its dynamic behaviour is studied via a switched system representation, where the state variables are the $N \cdot M$ phase currents and the output capacitor voltage V_c. However, to design the linear controllers of the ports a linearized model of the individual interleaved port is derived.

2.1 Switched model

The switched model is derived by the differential equations of each state of the converter, N-phases represents 2^N switching states as:

$$\begin{cases} \dfrac{d\,i_{L,ij}}{dt} = v_j - r_{lj}\,i_{L,j} - u_{ij}\left(r_{ds,j}\,i_{L,ij} + v_c + r_c\,C\,\dfrac{d\,v_c}{dt}\right) \\ \qquad\qquad -(1-u_{ij})\left(r_{f,j}\,i_{L,j} + v_{f,j}\right) \\ \qquad\qquad \vdots \\ \dfrac{d\,v_c}{dt} = \dfrac{1}{C\left(1+r_c\right)}\left(\sum_{j=1}^{M}\sum_{i=1}^{N} i_{L,ij}\,u_{ij} - \dfrac{v_c}{R_o}\right) \end{cases} \tag{1}$$

Where:

- v_j is the port input voltage.
- $r_{L,j}$, $r_{ds,j}$, $r_{f,j}$, $v_{f,j}$ are the port inductor resistance, transistor on-resistance, diode forward resistance and diode forward voltage respectively. It is assumed that the phases in a port have the same values.
- $i_{L,ij}$, $u_{ij,}$ the current and switching action of the phase i in port j.
- v_c the capacitor, and thus output voltage.

2.2 Linear average small-signal model

The linear average small-signal models are derived by the circuit analysis of the small-signal equivalent circuit of each interleaved port. The derivation of the transfer function of the interleaved converter has been derived already in [18] based on the equivalent averaged small-signal circuit shown in Figure 2 -2.

The voltage-to-duty ratio and inductor current-to-duty ratio transfer function are in the form:

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = G_v \frac{\left(1+\frac{s}{\omega_{z1,v}}\right)\left(1+\frac{s}{\omega_{z2,v}}\right)}{\frac{s^2}{\omega_0^2}+\frac{s}{Q\,\omega_0}+1} \tag{2}$$

$$\frac{\tilde{i}_L(s)}{\tilde{d}(s)} = G_i \frac{\left(1+\frac{s}{\omega_{z,i}}\right)}{\frac{s^2}{\omega_0^2}+\frac{s}{Q\,\omega_0}+1} \tag{3}$$

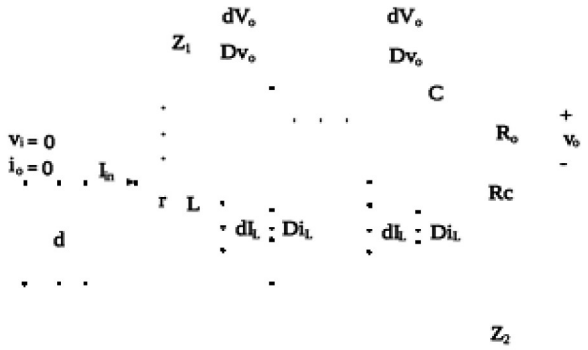


Figure 2-2 Averaged Small-Signal Model

3 Control design

The different control techniques are the building blocks, which generate the more complex control strategy of a MPC. Four of the most used control strategies in DC/DC converters are here briefly presented as basis for the study of the combined control strategies of the IMPC.

3.1 Voltage-mode control

The voltage-mode (VM) control requires sensing only the output voltage to achieve the purposes of voltage regulation. However, for energy management tasks, the IMPC requires to control also the current in one of the ports. As a result, the VM can find application to only one port.

A double lead-lag controller ensures in VM higher stability. The design of the double lead-lag controller is based on the K_{boost} approach presented in [20]. The double lead-lag controller boosts the phase in the bode plot at the required frequency via two zero at frequencies lower than the cut-off frequency (f_c) and reduces the phase via two poles above the f_c. As a result, the controller has a bell-shape phase plot at f_c.

The K_{boost} can be calculated as:

$$K_{boost} = \tan\left(45° + \frac{\phi_{boost}}{2n}\right)^{\square} \tag{4}$$

Where ϕ_{boost} is the amount of phase that needs to be boosted and n the order of the controller, two in the case of the VM. ϕ_{boost} usually needs to boost the phase drop due to an integrator in the controller at f=0, the phase-drop of the plant and the phase margin required (ϕ_m).

$$\phi_{boost} = -90° - \angle \frac{\tilde{v}_o(s)}{\tilde{d}(s)} \dot{c}_{f_c} + \phi_m \tag{5}$$

K_{boost} represents the geometric separation between poles and zeros of the controller to ensure the necessary ϕ_{boost}. Therefore, the frequency of the zeros f_z and of the poles can be calculated as:

$$f_z = \frac{f_c}{K_{boost}} \tag{6}$$

$$f_p = f_c K_{boost} \tag{7}$$

Finally, the double lead-lag controller has transfer function:

$$G_c = \frac{K_c}{s}\left(\frac{s+2\pi f_z}{s+2\pi f_p}\right)^n \tag{8}$$

Where K_c is the gain that ensures the required bandwidth to the closed-loop system.

3.2 Dual-loop control

The dual-loop control has an internal current-controlled loop that tracks the reference current and an outer-loop to track the reference voltage as shown in Figure 3 -3 where H_v and H_i are the voltage and current controllers respectively. The current-controlled loop can be used to control the energy flow from the source, but when combined with the outer loop the reference current is governed by the outer loop. As with the VM, this control strategy can be applied to only one port. The advantage of the dual loop is that it decouples the two loops and requires only a single lead-lag controller per loop. The single lead lag controllers can be designed based on (8).

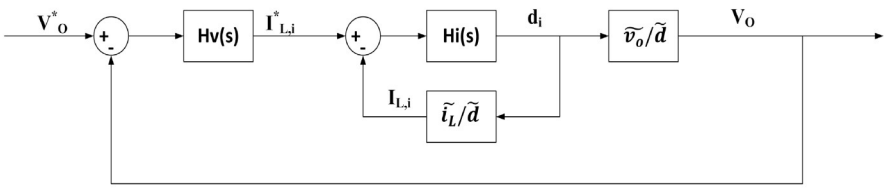


Figure 3-3 Dual-loop control

3.3 State-feedback control

The state-feedback control uses the matrices representation to design a controller for pole placement. The approach used to derive the state-space representation of the interleaved port follows [23]. The matrices A, B, C and D have the form:

$$A = \begin{bmatrix} -r/L & \frac{-1-D}{L} \\ n(1-D)C & \frac{-1}{R_o C} \end{bmatrix} \tag{9}$$

$$B=\begin{bmatrix} \frac{V_o}{L} \\ \frac{-nI_L}{C} \end{bmatrix} \tag{10}$$

$$C=\begin{bmatrix} 0 & 1 \end{bmatrix} \tag{11}$$

$$D=[0] \tag{12}$$

Where $r=r_L+Dr_{ds}+(1-D)r_f$ and $I_L=\frac{(1-D)V_o}{nR_o}$. The state feedback matrix K is computed based on the damping (ζ) and cut-off frequency required as:

$$K=Q^{-1}N \tag{13}$$

Where:

$$Q=\begin{bmatrix} b_1 & b_2 \\ a_{12}b_2-a_{22}b_1 & a_{21}b_1-a_{11}b_2 \end{bmatrix} \tag{14}$$

$$N=\begin{bmatrix} a_{11}+a_{22}+2\xi\omega_0 \\ \omega_0^2-a_{11}a_{22}-a_{12}a_{21} \end{bmatrix} \tag{15}$$

The inner transfer function is finally calculated as:

$$H_i=C\left(sI-ABK'\right)^{-1}B \tag{16}$$

At the outer loop, for voltage regulation, a simple PI controller is added designed via root locus.

3.4 Feedback-linearization control

The last control that will be investigated is the feedback linearization control. “Feedback linearization transforms a generic nonlinear model into a linear one by using a nonlinear feedback that cancels the original plant nonlinearity” [23]. The feedback-linearization is applied to the control port, which in this case is a 2-phases interleaved port and its linearization structure is shown in Figure 3 -4.

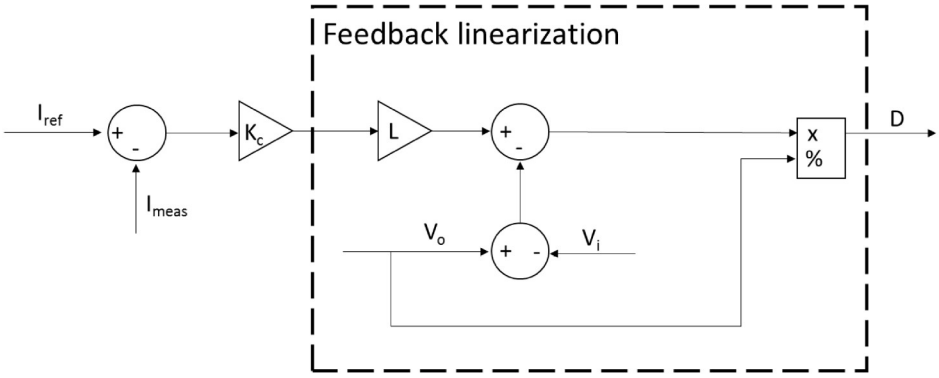


Figure 3-4 Feedback linearization structure

4 Comparative study of the control mix

The different control strategies are here combined and compared to evaluate the best solutions for automotive applications. The UC is voltage controlled and the battery is current controlled, both with bidirectional capabilities, the specifications of the MPC are given in Table 1. To each system is given the same set of disturbances and it is designed to respect the same bandwidth. The train step of disturbances is shown in Table 2, the step from 1.2 s to 1.4 s considers regenerative breaking mode with negative current from the load. Each converter is designed to have a 2 kHz bandwidth in order to avoid amplification of the ripple due to the switching frequency of the converter 20 kHz. However, this condition is not always achievable as will be shown in the next sections. As no energy management is designed in this paper, the current reference to the current controlled port is simply defined as $I^{¿} = \frac{P_o}{V_{¿}}$, assuming no losses in the converter.

Table 1 MPC Characteristics

MPC Characteristics	**UC Port**	**Battery port**
Input voltage	250 V	200 V
Number of phases	3	2
Inductance	100 uH	200 uH
Inductor resistance	17 mΩ	34 mΩ
IGBT on-resistance	7.5 mΩ	7.5 mΩ
Diode forward resistance	6.5 mΩ	6.5 mΩ
Switching frequency	20 kHz	20 kHz

Table 2 Train disturbances on the converter

Time [s]	**0.2**	**0.3**	**0.4**	**0.5**	**0.6**	**0.7**	**0.8**	**1.0**	**1.2**	**1.4**
Step	$V_{i,1}$ -10%	$V_{i,1}$ +10 %	$V_{i,2}$ -10%	$V_{i,2}$ +10 %	V_o +10 %	V_o +10 %	I_o +100%	I_o -100%	I_o -200%	I_o +200%

4.1 Port Interleaving

An MPC with parallel ports has a common DC capacitor for the different ports as shown in Figure 1 -1. The DC capacitor serves as a buffer to supply with a ripple-free voltage the load. However, in an MPC the capacitor needs to carry the output currents from several ports resulting in lower filtering capabilities. A port interleaving concept is here introduced to reduce the peak current and the voltage ripple at the DC-link. More generally, each converter benefits already from the phase interleaving, therefore a general expression of the phase switch can be drawn.

$$\phi_{i,j} = (i-1)\phi_m + (j-1)\phi_{n_i} \quad \text{for} \quad 1 \le i \le m \quad , \quad 1 \le j \le n_i \tag{17}$$

Where:

$$\phi_m = \frac{360°}{m} \tag{18}$$

$$\phi_{n_i} = \frac{360°}{n_i} \tag{19}$$

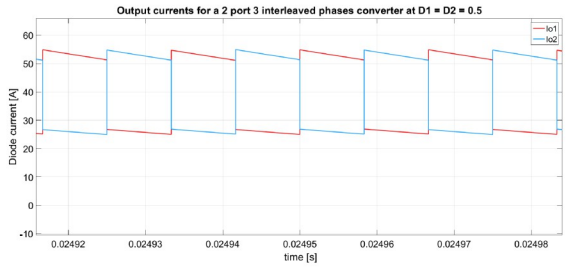
The value m and n_i express the number of parallel ports and phases for the corresponding i-port respectively.

By shifting the switches based on equation (18) and (19) the output currents are shifted as can be seen in Error: Reference source not found(a).

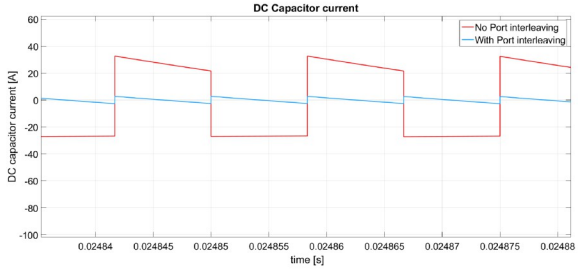
The current flowing in the DC capacitor (I_C) is:

$$I_C = \sum_{i=1}^{m} I_{o,i} - I_{Load} \tag{20}$$

Where $I_{o,i}$ is the output current for the given port and I_{Load} the load current. Thanks to the port shifting the DC capacitor current can be decreased as can be seen in Error: Reference source not found(b). In fact, the output current per port is the sum of the interleaved diode currents, the port shift allows to don't inject in the capacitor the maximum output current at the same moment. As a result, the voltage ripple at the DC link is significantly decreased as can be seen in Error: Reference source not found(c).



(a)



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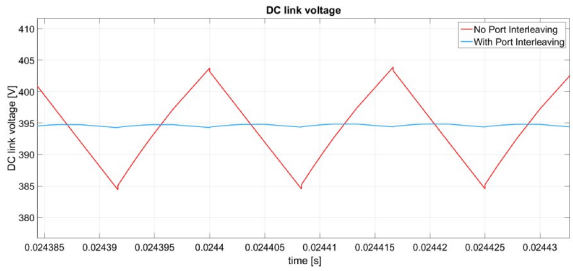
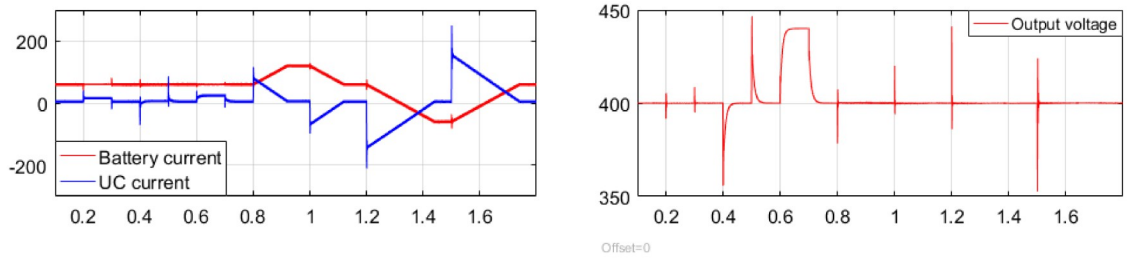


(c)

Figure 4-5 Unfiltered output port currents, (b) DC capacitor current, (c) DC-bus voltage

4.2 Voltage mode control and Current mode control

In the voltage mode control, a 2 kHz bandwidth will force the system to instability due to relatively low gain margin. On the other hand, the cut-off frequency should be above the natural frequency of the system, here equal to 964 Hz. As it is clear, only a small portion of the frequency range is available for the selection of the cut-off frequency. Therefore, the voltage mode controller is designed for a bandwidth of 1.2 kHz. The current-mode controller is designed to have a 2 kHz bandwidth. The response of the battery/UC current and output voltage is given in Figure 4 -6.

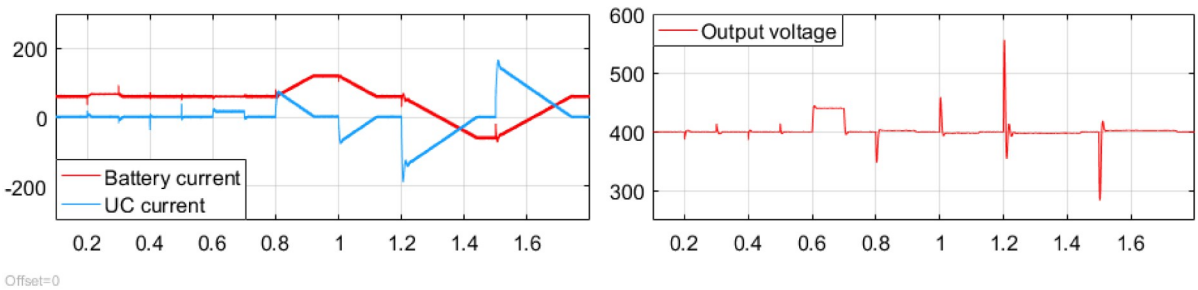


(a) (b)

Figure 4-6 Voltage-mode and Current-mode control: (a) Input currents response, (b) output voltage response

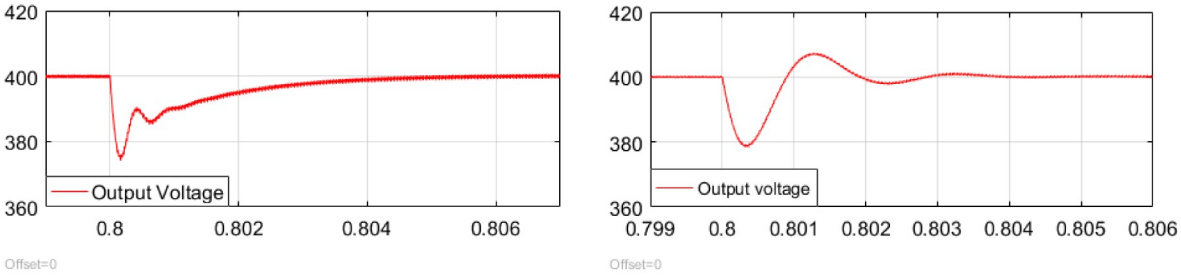
4.3 Dual-loop and Current mode control

The combination of dual-loop control and current mode control has been successfully applied to MPC topologies as in [4]. The advantage of this method relies on a simpler design of the two nested controllers. Both the inner and outer controllers are single lead-lag controllers. However, the dynamics of the two loops need to be clearly separated resulting in a slower outer loop. In fact, since the current controller is designed at 2 kHz, the voltage controller needs to have a bandwidth lower than 200 Hz. As a result, the voltage response to a load step is slower compared to the voltage mode case, causing higher output voltage peaks as can be seen in Figure 4 -7b at the step occurring at 1.2 s. However, more stable, thanks to the inner control as can be seen from the minor ringing in the dual-loop compared to the voltage-mode control as can be seen in Figure 4 -8.



(a) (b)

Figure 4-7 Dual-loop and Current-mode control: (a) Input currents response, (b) output voltage response

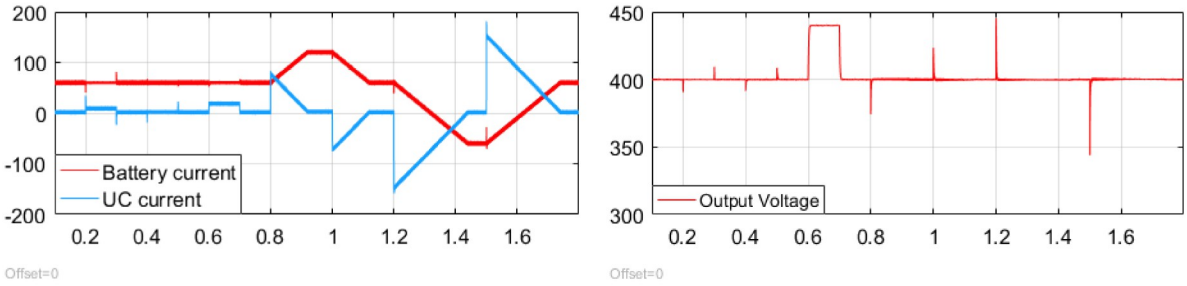


(a) (b)

Figure 4-8 Voltage response to the load step at 0.8s: (a) Voltage-mode control (b) Dual-loop control

4.4 State-feedback and Current mode control

In the case, the UC port is controlled with state-feedback control both the current and the voltages are jointly controlled at 2 kHz. As a result, the voltage response is faster compared to the case of voltage-mode and dual loop control, resulting in a lower peak voltage value as can be seen in Figure 4 -9.



(a) (b)

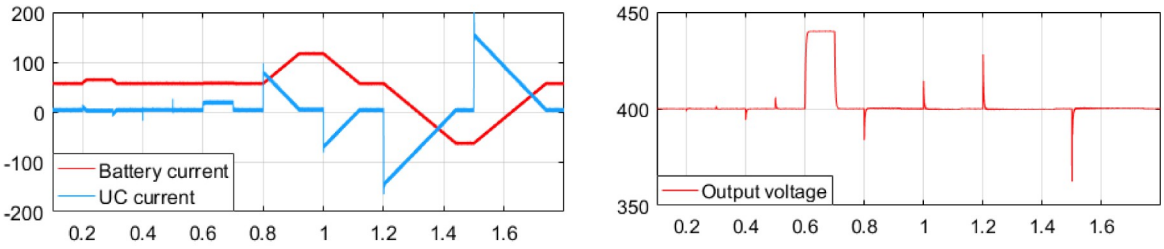
Figure 4-9 State-feedback and Current-mode control: (a) Input currents response, (b) output voltage response

4.5 State-feedback and Feedback linearization current controlled

In [23], a feedback linearization control is applied on a flyback converter with a PI outer-loop control. The design of the PI in the outer-loop is sensitive to μ, which is a hyper-parameter to tune for governing the voltage response. However, in a MPC the voltage can be controlled by one of the ports, relieving the second port to voltage regulation tasks. As a result, it is possible to exploit the advantages of linearizing the current control port for better performances on the current port. Figure 4 -10, presents the responses of the

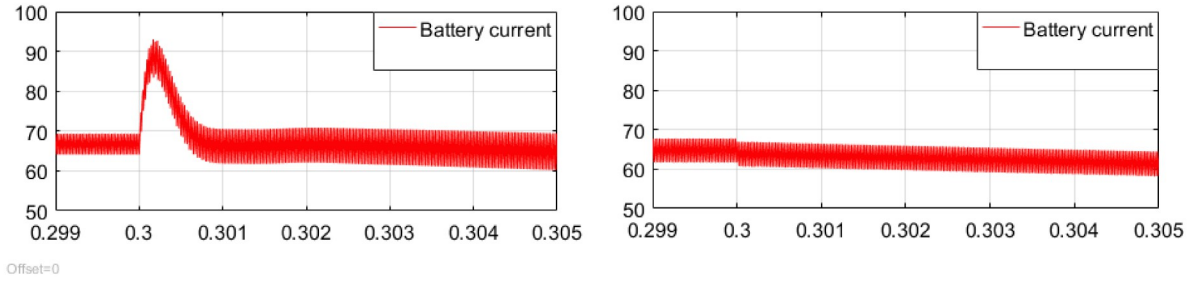
output voltage and sources current. It is worth to note the smoother behaviour of the battery current with feedback-linearization compared to the dual loop case as shown in Figure 4 -11.

The disadvantage of feedback linearization is its sensitivity to parameter estimation. However, an incorrect parameter estimation does not play a significant role when the port is current controlled and sustained by a second port voltage controlled. In fact, by giving a false estimation of the inductance to one of the phases, the controller is still able to accomplish its task of current regulation.



(a) (b)

Figure 4-10 State-feedback and Current feedback-linearization control: (a) Input currents response, (b) output voltage response



(a) (b)

Figure 4-11 Battery current response to input voltage drop: (a) Current mode control, (b) Feedback linearization control

5 Discussion

The most promising control mix is the combination of state-feedback control for the voltage port and feedback linearization for the current port. The advantage of a fast response in the voltage given by the state-feedback control is combined with the advantage of a linearized system in the current port. In this section, the standard dual-loop control and current-mode (DL-CM) control is compared with the mix state-feedback/feedback-linearization control (SF-FL). As the current reference is subjected to a slope for the battery port, instead of a step, the authors decided to examine the control mix in terms of its capability to reject disturbances. The peak immediately after the disturbance expresses how fast the controller will counteract, a lower peak expresses a faster response. On the other hand, the output voltage will have a steady-state error while the battery current is rising, overshoot is taken into account. As it is clear from Table 3 the SF-FL control outperforms the DL-CM. The FL ensures smooth variations of the current, leaving the UC to deliver the rest of the required power. As a result, the current in the UC bank with SF-FL control is higher when compared to DL-CM. The disturbances also shown in Table 2 are given to an initial condition of $V_{i,1}$ = 250 V, $V_{i,2}$ = 200 V, V_o = 400 V and P_o=15 kW.

Table 3 Response peaks comparison between DL-CM and SF-FL

	Step1	**Step3**	**Step**	**Step7**	**Step9**	**Step11**

5

DL-CM	Battery Current	Response peak	-25 A	+12 A	-8 A	+21 A	-30 A	+40 A
	UC Current	Response peak	+18 A	-35 A	+26A	+78 A	-190 A	+167 A
	Output Voltage	Response peak	- 13V	-13.5 V	0 V	-52 V	+156 V	-116 V
		Overshoot peak	+3 V	+3V	+ 4 V	+4V	-46V	+18.5 V
SF-FL	Battery Current	Response peak	+1 A	0 A	0 A	0 A	0 A	-1 A
	UC Current	Response peak	+15 A	-18 A	+21A	+95 A	-165 A	+215 A
	Output Voltage	Response peak	- 1.5 V	-6 V	0 V	-16 V	+28V	-38.5 V
		Overshoot peak	+0.5 V	0 V	0 V	0 V	0 V	0 V

6 Conclusion

In this paper, the control designs of different control techniques are developed. The various advantages and drawbacks of each control techniques have been evaluated. The preliminary results show the advantage of state feedback control for the voltage controlled port ensuring fast disturbance rejection. In addition, feedback linearization applied to the current port keeps the current far from abrupt changes due to the disturbances in the voltage and in the load, preserving therefore its lifetime. The port interleaving concept has been also introduced to decrease the voltage ripple at the capacitor side.

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