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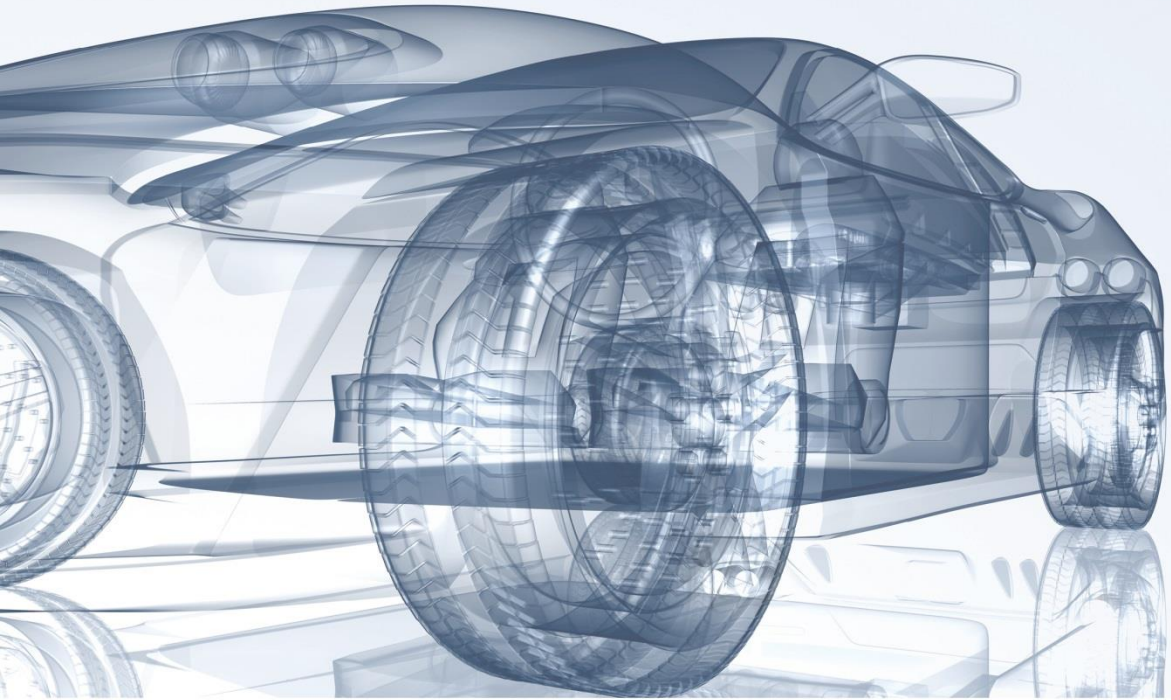

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Cycle Life Evaluation of Lithium-Ion Capacitors

Agenda

- Background and contribution
- Test conditions
- Load profiles
- Experimental results
- Conclusion

Background and contribution

1. Having an accurate model of life prediction can significantly accelerate the penetration of LIC technologies in various applications.

2. The lifespan of the LIC is subject to decrease due to the capacity fade and internal resistance rise during cycling and calendar aging processes.
   - Cycle life : is influenced by C-rate, DOD, and other conditions. Typically, higher DOD corresponds to a lower cycle life.
   - Calendar life : There are three key factors that influence calendar life i.e. Temperature, Time and SOC.

3. As there are a few models published in the literature about LIC lifetime model ➔ we are encouraged to establish an accurate lifetime model for a wide range of application.

4. The first step to have a lifetime model is to investigate the capacity degradation trend and internal resistance increase at different conditions.

Test conditions

- 18 cells are devoted for lifetime modeling.
- For calendar test, 9 cells are stored at different temperatures with different SOCs. The capacity fade and internal resistance rise is measured every month.
- For cycling aging test, 9 cells are cycled at different temperature with different load profiles. Load profiles are different in regard of current level and DOD.

Cycling tests conditions and test profiles

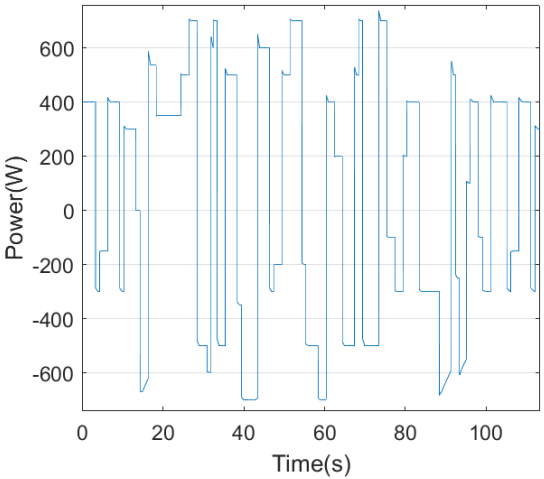
Cell number	Cycling profile	RMS value (W)	Temperature (°C)
1, 4, 7	HD	479	0, 25, 45
2, 5, 8	HD RMS	280	
3, 6, 9	LD	148.15	

Calendar test conditions

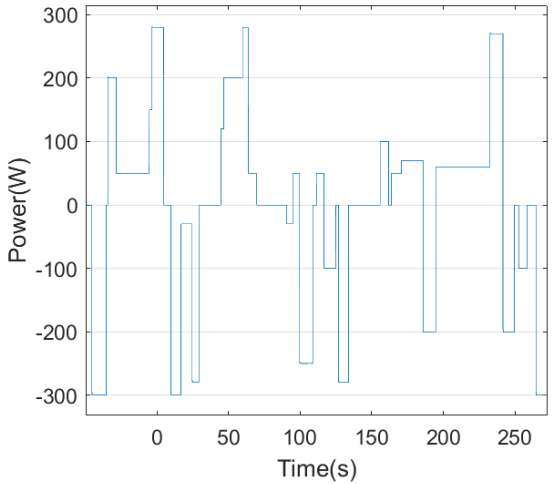
Cell number	SOC (%)	Temperature (°C)
10, 13, 16	0	0, 25, 45
11, 14, 17	50	
12, 15, 18	100	

Load profiles

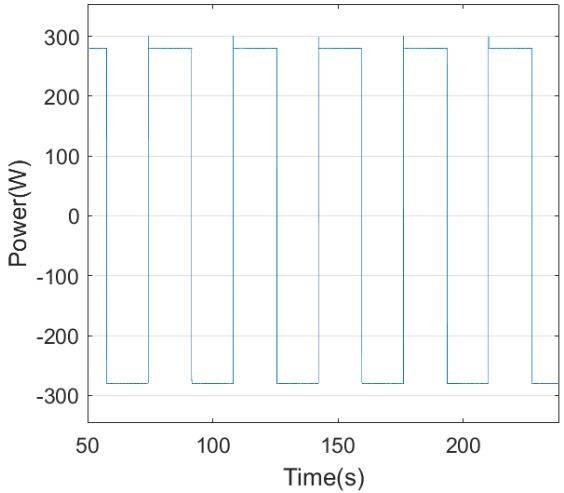
Heavy duty (HD) load profile



Low duty (LD) load profile

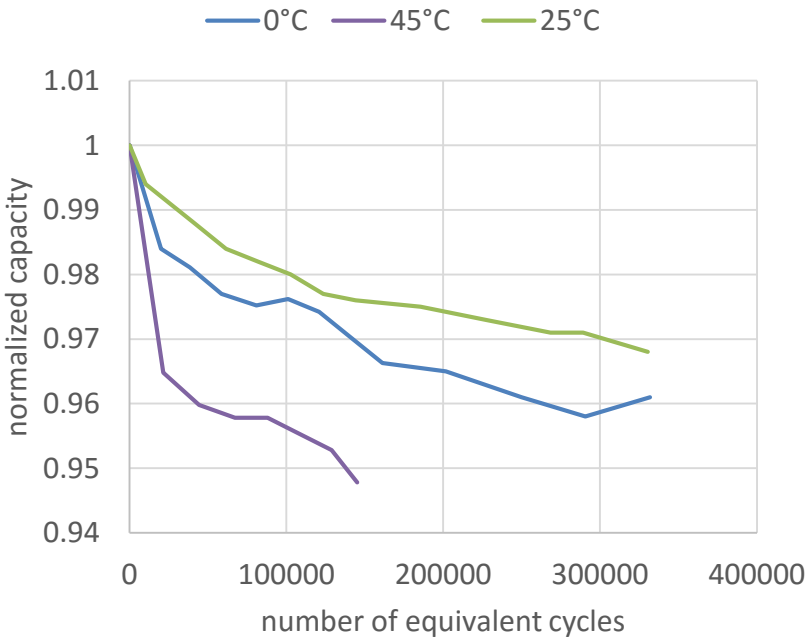


HD (RMS) load profile

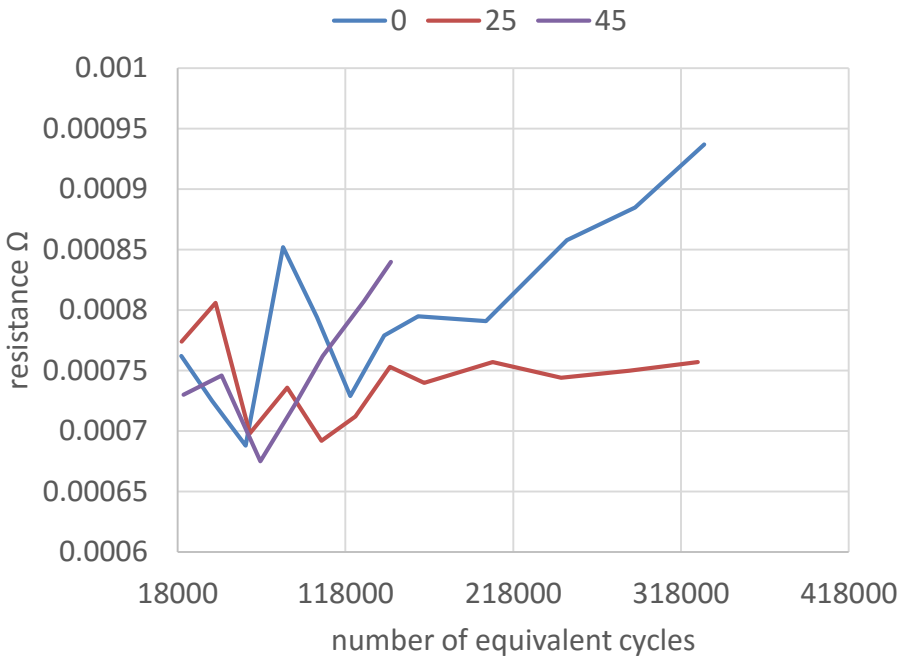


Experimental result (HD)

Capacity/initial capacity

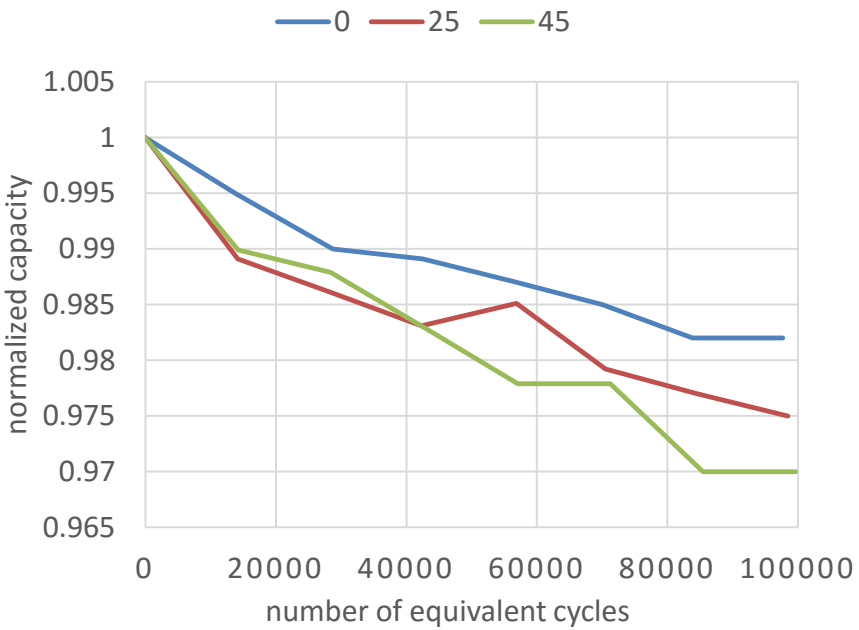


Internal resistance

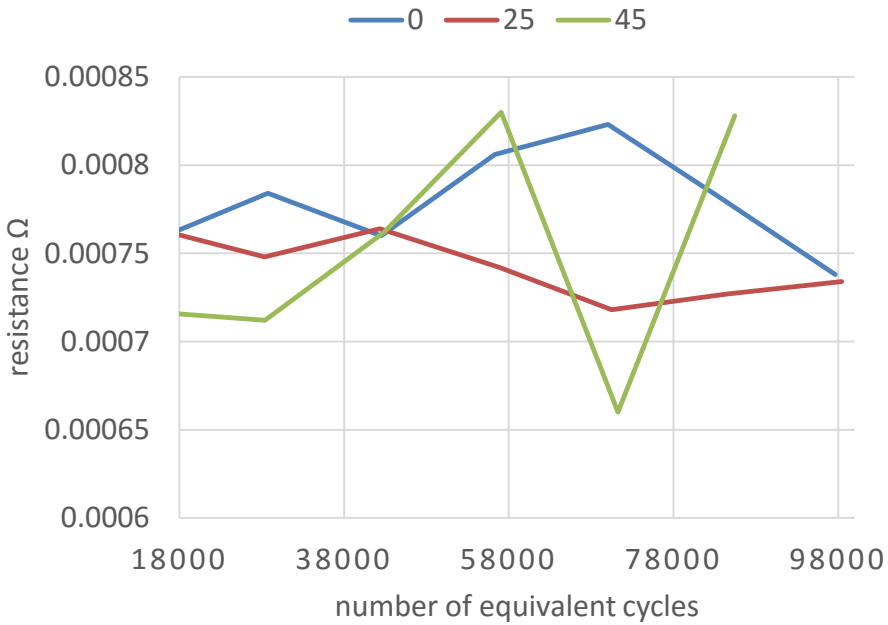


Experimental result (LD)

Capacity/initial capacity

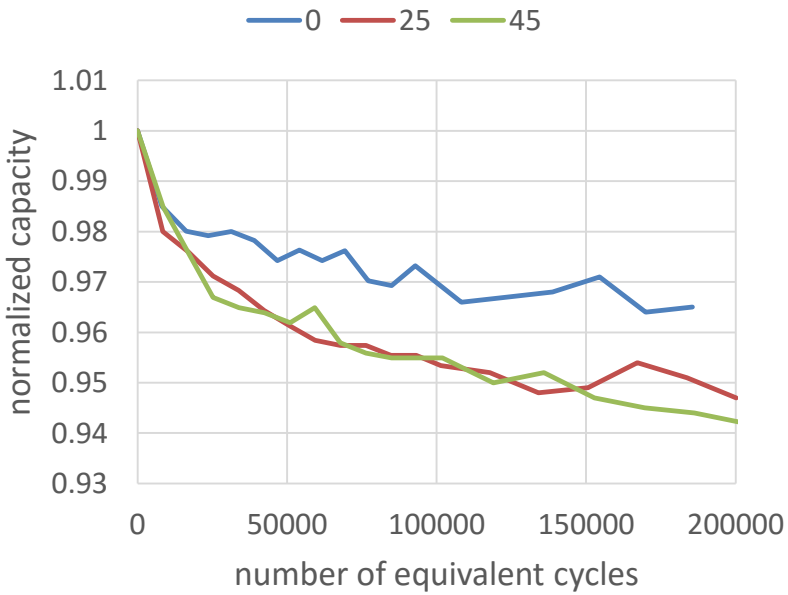


Internal resistance

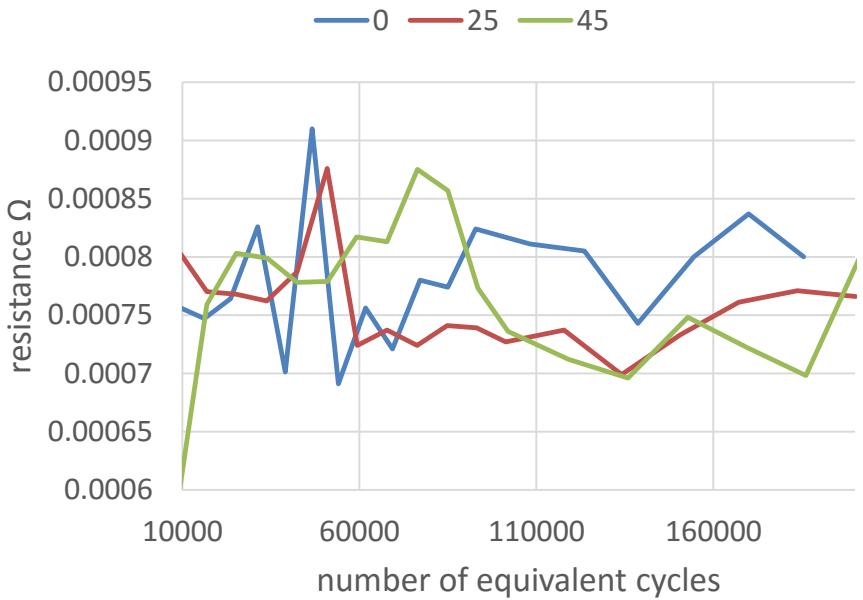


Experimental result (HD (RMS))

Capacity/initial capacity

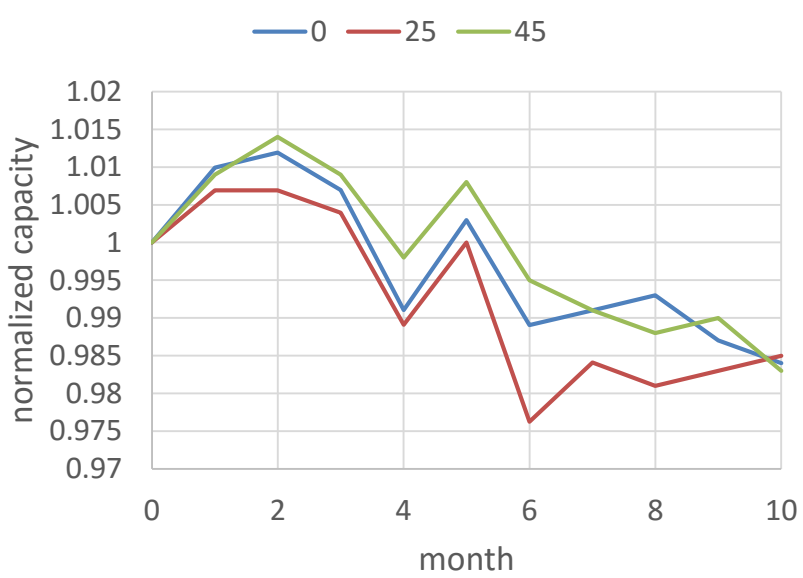


Internal resistance

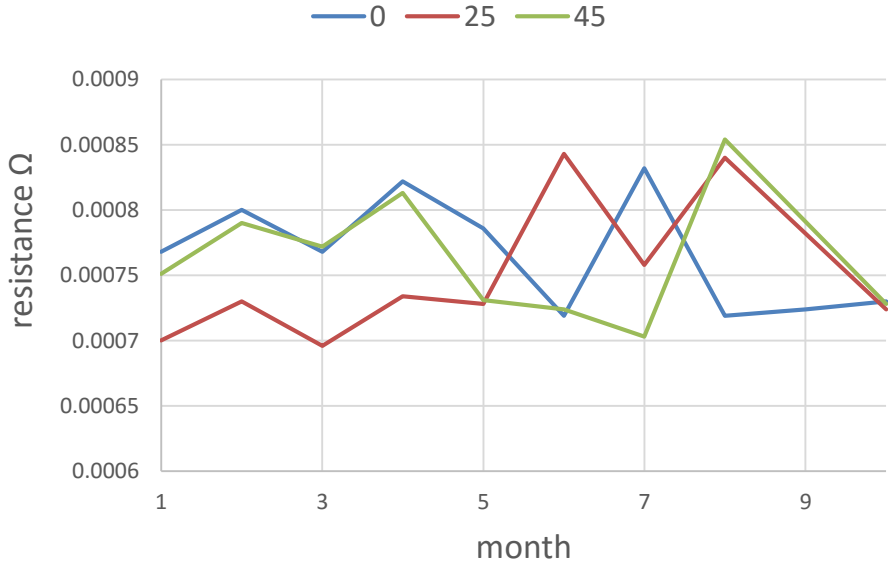


Experimental result (calendar aging tests, 100% SOC)

Capacity/initial capacity

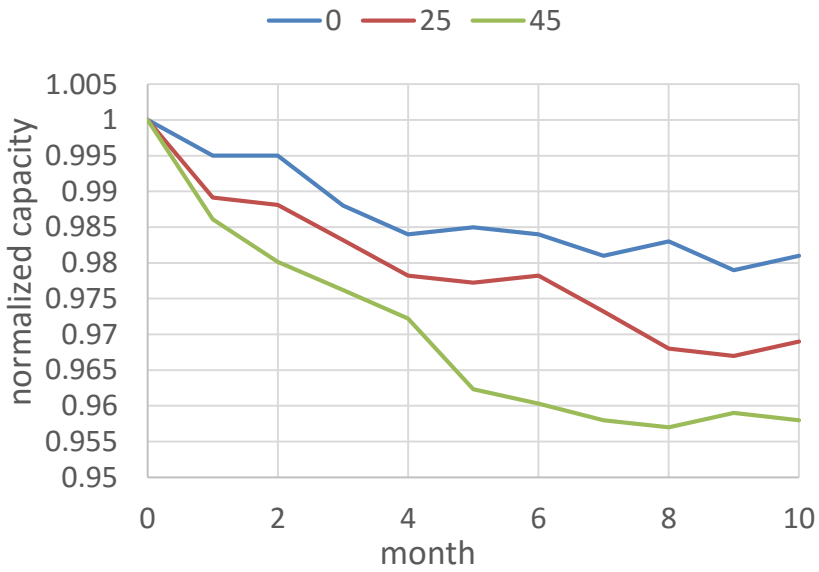


Internal resistance

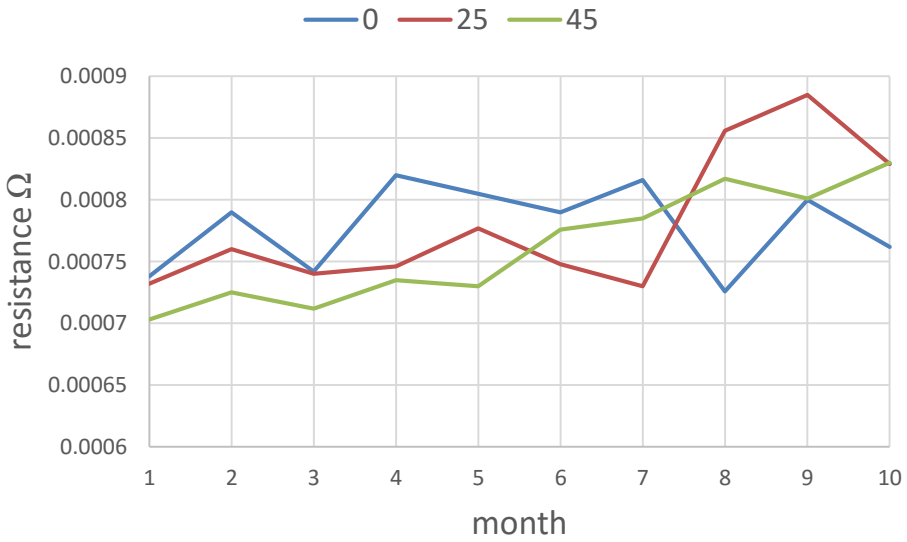


Experimental result (calendar aging tests, 50% SOC)

Capacity/initial capacity

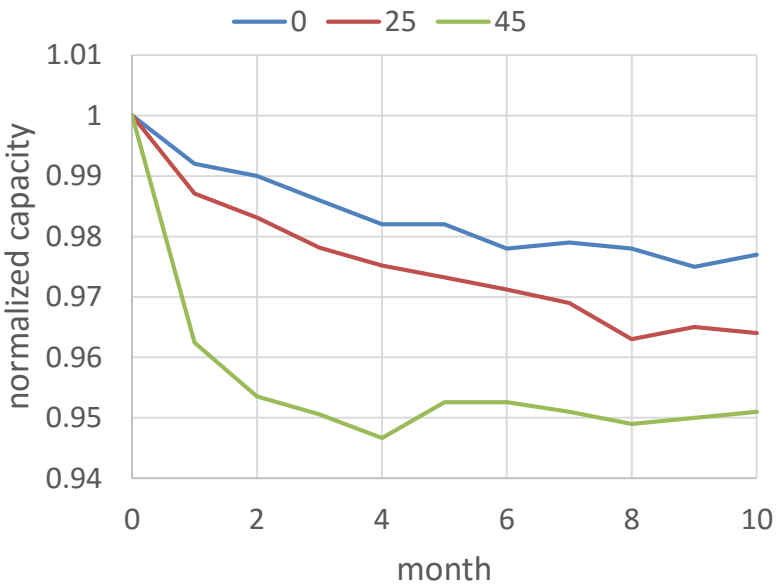


Internal resistance

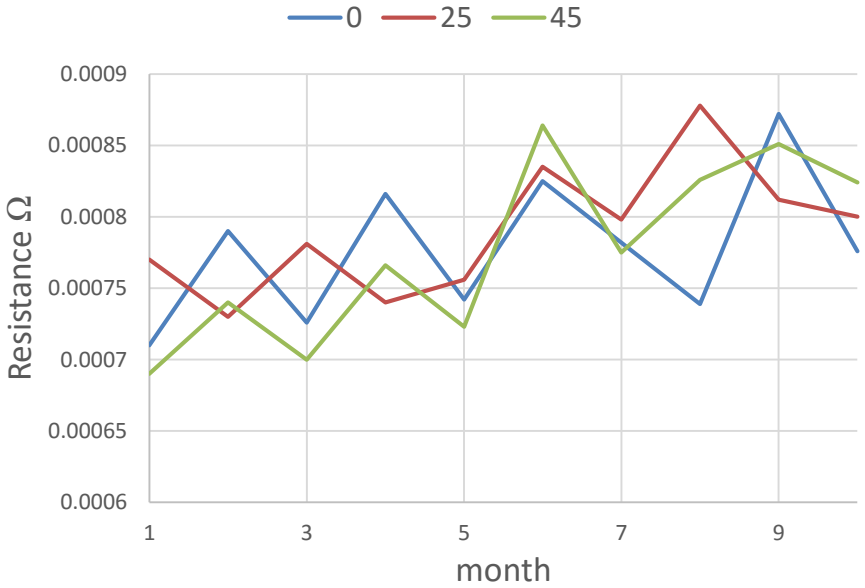


Experimental result (calendar aging tests, 0% SOC)

Capacity/initial capacity



Internal resistance



Conclusion

- The higher the temperature is, the more the LICs is deteriorated, implying that aging can be accelerated by elevated temperatures.
- DOD which corresponds to the current level and load duration, has a significant effect on Internal resistance. The higher DOD, the higher increase in internal resistance.
- A higher current tends to a higher capacity fade. However, the effect of current on the capacity is not significant.
- For storage, in regards of capacity fade, storage at 45°C with 100% SOC is the best condition. in this SOC, the internal resistance doesn't change.
- For storage at lower SOC, 0°C is the most favorable temperature. Although the internal resistance increases significantly.
- The worst condition for storage is 0% SOC at 45°C.

Thank you for your attention