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Design and test of a battery pack simulator

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Abstract

This paper describes the design of a battery pack simulator (BPS). The BPS is an electronic device that emulates all cell voltages of a battery pack in order to test battery management systems (BMS). Cell characteristics and environmental conditions of individual cells, such as capacity or ambient temperature can be adjusted in order to examine the unbalance in a battery pack on the functioning of the BMS. The BPS implements a real time simulation model that comprises interacting electric and thermal submodels. The BPS uses xPC Target and Simulink as real-time software environment. A hardware interface converts all simulated cell voltages and temperatures to real voltages that can be connected to the voltage and temperature sensor inputs of a BMS. We have tested the BPS by comparing the emulated cell voltages of it to the cell voltages of a real battery pack that consists of $LiFePO_4$ cells. In order to do so, a thermal cell model and third order equivalent network model has been derived by analysing EIS-measurements and pulse current measurements. The found network is implemented in the BPS. Test results show that the maximum deviation between the real and emulated cell voltages is at most 0.5%. We have connected our BPS to a Lithiumate Pro BMS and evaluated the capability to test it with our BPS. We found that basis functionality, like SoC estimation and over and under voltage detection could be tested well. At this moment, the BPS is not suited to test the balancing feature of BMS. Further development of the BPS is needed to enable the testing of this feature of BMS as well.

Keywords: BMS (Battery Management System), modeling, hardware-in-the-loop (HIL)

1 Introduction

The testing and evaluation of battery management systems (BMS) is in practice an awkward and time consuming activity. A complete test includes temperature tests, tests of unbalances in battery packs, tests of unknown initial state of charge values, and so on [1]. Also, it is often difficult to test the BMS in a laboratory with the same load and environmental conditions that a battery pack might face in practice. In order to facilitate the testing of BMS we have designed a battery pack simulator (BPS). The BPS is an electronic device that emulates all cell voltages of a battery pack under various adjustable battery conditions. The

BPS can be used also for testing voltage management systems of fuel cell stacks.
The BPS calculates the voltages and temperatures of all cells in a battery pack that consists of at most 248 cells. The user can define his own battery model, so batteries with different cell chemistries can be emulated. Cell characteristics and environmental conditions of individual cells, such as capacity or ambient temperature can be adjusted in order to test the impact of unbalance in a battery pack on the functioning of the BMS. The BPS implements a real time simulation model that comprises interacting electric and thermal submodels. A hardware interface converts all simulated cell voltages and temperatures to real voltages that can be connected to the voltage and temperature sensor inputs of a BMS.
This paper explains the architecture of the battery simulator, the hardware interface, the modeling of a battery pack that consists of $LiFePO_4$ cells and the basic testing of an Elithion Lithiumate PRO BMS by using our BPS.

2 Architecture of battery pack simulator

The hardware of the BPS consists of four main components (Fig.1): a host PC, an xPC target, a FGPA board and a set of at most 64 isolation amplifiers.

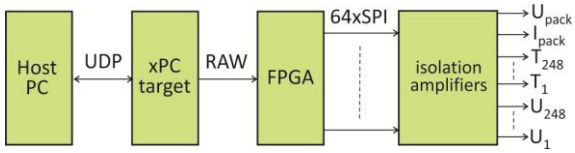

Figure1: Block diagram of the battery pack simulator

The Host PC is the interface between the user and the model. The host PC enables the user to start or stop a simulation, watch simulation results and to enter the model input.

The battery model runs on an xPC target and exists in outlines of four subsystems (Fig.2):
1. The subsystem ‘UDP data from host’ handles the model input that is sent from the host to the xPC target. The model input consists of the battery current and adjustable cell parameters and variables. The model in Fig.2 defines 5 adjustable cell parameters, but this can be expanded according to the user’s needs. Port numbers of the UDP packets are used to identify the adjustable variables and parameters in order to support flexible and easy configurable model implementations.

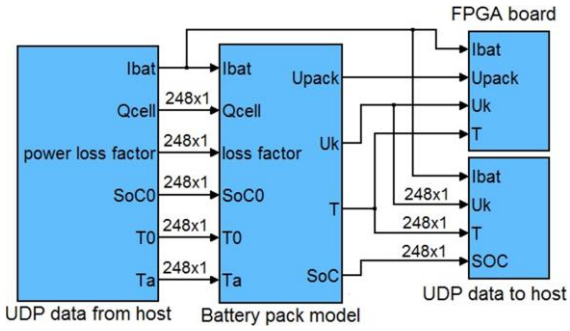

Figure2: Block scheme of the model that runs on the xPC target

2. The subsystem ‘UDP data to host’ handles the model output that is sent from the xPC to the host. The model output consists of terminal voltages, temperatures and state of charge of all cells.
3. The subsystem ‘Battery pack model’ defines the cell and battery pack model and is discussed in more details later in this paper.
4. The subsystem ‘FPGA board’ provides the model output that is sent to the FPGA board. The model output to the FPGA board holds 512 variables. In the configuration, shown in Fig.1, the output consists of 248 cell voltages, 248 cell temperatures, the battery pack voltage, a current sensor output. Zero value placeholders are used if the battery pack consists of less than 248 cells. All simulated output variables are scaled to 16-bit variables that can be processed by the digital to analog converters (dac’s) in the isolation amplifiers. An offset calibration feature is implemented to correct offset error(s) that may arise in the analog signal processing circuit.
Raw datagrams are used for the communication between the xPC and FPGA because of its fast and rather simple protocol.

The FPGA board is the interface between the xPC target and the isolation amplifiers. The FPGA is responsible for receiving and decoding the Raw datagram packets sent by the xPC target. The FPGA decomposes the 512 output variables into 64 sets of 8 variables that are transmitted to isolation amplifiers circuits by 64 SPI busses. All 64 SPI busses share the same clock- and latch signal in order to limit the number of signals and to provide synchronous sampling. Each SPI bus has its own data signal. The SPI busses are connected to isolation amplifiers. Each isolation amplifier circuit provides eight analog voltages

that can be configured to represent cell voltages, temperature sensor signals or a combination of both. The isolation amplifiers provide the analog voltages that can be connected to the BMS cell voltage inputs or temperature or current sensor inputs. Its working is discussed in the next section.

3 Isolation amplifier circuit

Fig.3 shows the functional block scheme of the isolation amplifier circuit. The SPI-bus operates at a bit rate of 500 [kbit/s]. The chosen bit rate limits the maximum sample rate to at most 3.9 [kSamples/s] (=[500kbits/s] / (8 words * 16 bits)). The SPI signal are galvanic isolated from the FPGA board by optocouplers. The secondary sides of the optocouplers are connected to 8 daisy-chained 12-bit dac's. The dac's are grouped in two sets of four isolation amplifiers that share a common power supply. An analog processing circuit converts the voltages of the dac's to output voltages. The design of the analog circuit allows the following configurations:

- Configuration 1 is applicable to emulate the cell voltages of eight subsequent cells when the BMS under test uses multiple cell monitor units. Then, it applies: $U_{out1} = U_{adc1}$, $U_{out2} = U_{out1} + U_{adc2}$, $U_{out3} = U_{out2} + U_{adc3}$ and so on.
The gnd2 connection of the upper analog process circuit must be connected to U_{out4} of the lower analog process circuit.
- Configuration 2 is applicable to emulate the temperature sensor voltages of eight subsequent temperature sensors when the monitor unit of the BMS under test uses analog temperature sensors with a common ground. In that case, it applies:
$U_{out1} = U_{adc1}$, $U_{out2} = U_{adc2}$, $U_{out3} = U_{adc3}$ and so on.
The gnd2 connection of the upper analog process circuit must be connected to gnd1 of the lower analog process circuit.
- Configuration 3 is applicable to emulate the cell voltages when the BMS under test uses single cell monitor units. In that case, the outputs emulate alternately cell voltage and temperature sensor signals of four subsequent cells. it applies:
$U_{out1} = U_{adc1}$ (voltage ofcell 1),
$U_{out2} = U_{adc2}$ (temperature sensor voltage cell 1)
$U_{out3} = U_{out1} + U_{adc3}$ (voltage of cell 2)
$U_{out4} = U_{out1} + U_{adc4}$ (temperature sensor voltage cell 2)
$U_{out5} = U_{out3} + U_{adc5}$ (voltage cell 3)
$U_{out6} = U_{out3} + U_{adc6}$ (temperature sensor voltage cell 3)
$U_{out7} = U_{out5} + U_{adc3}$ (cell voltage cell 4)
$U_{out4} = U_{out5} + U_{adc8}$ (temperature sensor voltage cell 4)
The gnd2 connection of the upper analog process circuit must be connected to U_{out3} of the lower analog process circuit.

The maximum output current of the emulated voltages is limited to 30 [mA]. This is an important restriction that makes the BPS not suited to test the balancing feature of a BMS.

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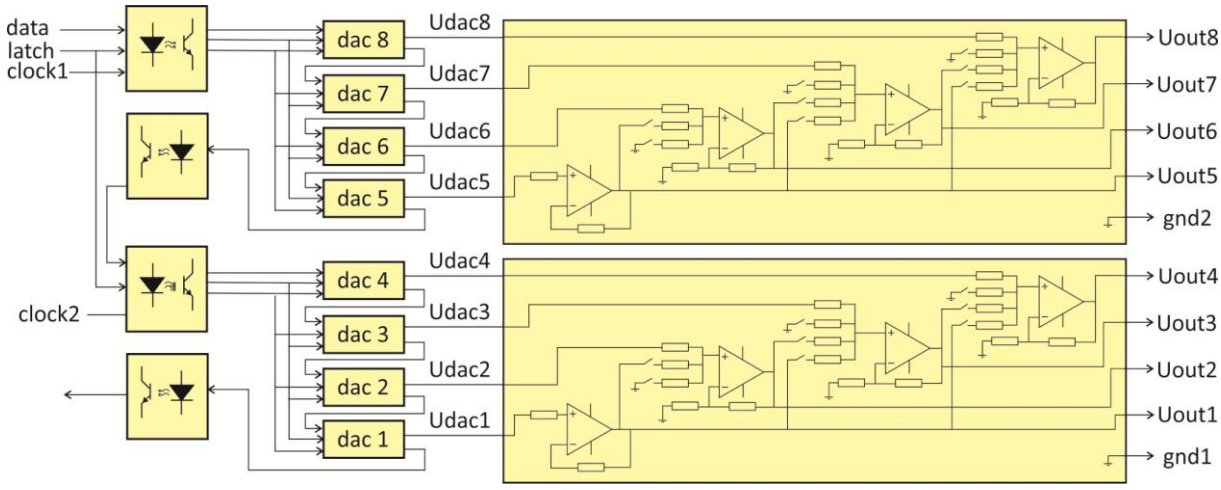

Figure3: Functional block scheme of the isolation amplifiers

4 Battery pack model

In this section we discuss the battery pack model subsystem (see Fig.2). This subsystem calculates the cell voltages and temperatures of all cells of a battery pack. In principle, the user may define any cell modeling method such as analytical, electrochemical or electric circuit model techniques that can be implemented in Simulink.
In this paper we focus on the cell modeling by means of electric circuit models because of its relative simplicity. A simple model is preferable because the model must be calculated real time for each cell.

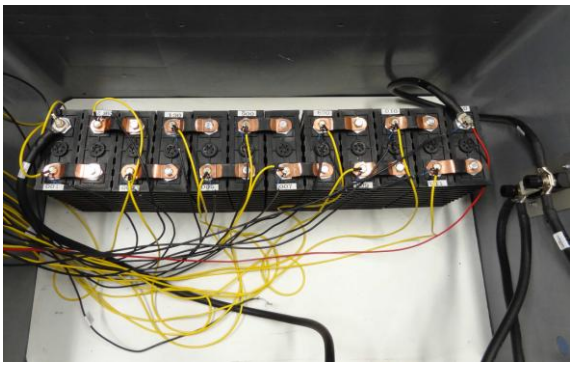

Figure4: Battery pack that consists of 12 cells.

In this paper we describe the modeling of a battery pack that consists of twelve 100 [Ah] Sinopoly $LiFePO_4$ cells. The 12 cells were placed in one row (see Fig.4.).

4.1 Thermal submodel

The thermal model of the battery pack is based on the thermal heat conductance between the cells mutually and from the cells to the environment [2], [3], [4]. We used equation 1 to determine the cell temperatures.

$$T_i = T_i^0 + \frac{1}{C_{th}} \int \left(P_i + \kappa_i^{ca} \cdot (T_i^a - T_i) + \sum_{j=1, j \neq i}^{Ncells} \kappa_{ij}^{cc} \cdot (T_j - T_i) \right) dt \qquad (1)$$

where: T_i^0 = initial temperature of cell i, C_{th} = heat capacity of cell, P_i = heat dissipation in cell i, κ_i^{ca} = heat conduction coefficient from cell i to ambient, T_i^a = ambient temperature of cell i, κ_{ij}^{cc}= heat conduction coefficient from cell i to cell j.

The heat production of cell i consists of a part that arises from the entropy change of the reaction and a part caused by the overpotential voltage. In our model it is calculated as [5]:

$$P_i = I \cdot (U_{ocv,i} - U_{t,i})$$

U_{ocv} = open terminal voltage of cell i and $U_{t,i}$ = terminal voltage of cell i.

We did not take the reversible heat effect into account.

We measured the heat capacity of a cell by means of a calorimeter and found a value of:

C_{heat} = 4090 [J/K].

This corresponds to a specific heat capacity of 1.3 [$J \cdot g^{-1} \cdot K^{-1}$]. This is 15% more than reported by [6].

The heat conduction coefficients have been determined by measuring the stationary temperature rise of all cells when the pack is loaded by an 80 [A] alternating charge / discharge current (see Fig.5).

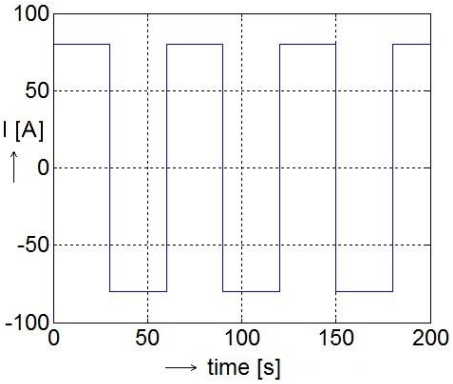

Figure5: Symmetrical charge/discharge current that is used to heat up the battery cells.

Because of the symmetry of the current, the average internal power loss in the cell can be calculated as:

$$P_i = 80\,[A] \cdot \frac{1}{T} \cdot \int_0^T U_i \cdot sign(I) \cdot dt \qquad (2)$$

where: U_i = terminal cell voltage of cell i, T = period time of current.

Table 1 lists the average power losses and temperature rise of each cell.

Table1: Power losses and temperature rises of the cells due to an alternating 80[A] charge/discharge current.

cell nr.	1	2	3	4	5	6
P_i [W]	4.1	4.3	4.4	4.1	4.5	4.5
ΔT_i [°C]	9.4	11.5	12.5	13.2	13.1	13.4
cell nr.	7	8	9	10	11	12
P_i [W]	4.3	4.5	4.2	4.7	4.3	4.7
ΔT_i [°C]	13.4	13.2	13.7	13.3	11.6	9.7

Based on the construction of the battery pack, we assume three independent heat conduction coefficients. These are:
κ_1^{ca}: the heat conduction coefficient of cell 1 and 12 (the cells on the edge of the pack) to ambient
κ_2^{ca}: the heat conduction coefficient of all cells but cell 1 and 12 to ambient
κ_{ij}^{cc}: the heat conduction coefficient between two adjacent cells (i=j+1 or i=j-1).
The heat conduction coefficients of non-adjacent cells are assumed to be 0.

The three heat conduction coefficients κ_1^{ca}, κ_2^{ca} and κ_{ij}^{cc} were determined by least squares fitting of the data of table 1 and the equation 3.

$$P_i = \kappa_i^{ca} \cdot \Delta T_i^a + \sum_{j=1, j\neq i}^{Ncells} \kappa_{ij}^{cc} \cdot \left(\Delta T_i - \Delta T_j\right) \qquad (3)$$

We found the following values:

κ_1^{ca} = 0.47 [W/K]
κ_2^{ca} = 0.34 [W/K]
κ_{ij}^{cc} = 0.06 [W/K]

4.2 Electric submodel

In order to determine the electric model, we have executed three kinds of measurements:
1. Open terminal voltage measurements
2. EIS-plot measurements
3. Current pulse measurements

4.2.1 Open terminal voltage measurements

We measured the terminal voltage during a C/50 charge and discharge current at temperatures of T=0[°C], T=25[°C] and T=40[°C]. Fig.6 shows the measurement results. The graphs show a clear hysteresis effect that increases at low temperatures. This effect has also been reported in literature [7], [8]. In our model we didn't include the hysteresis effect. We used the average value of the terminal voltage of the charge and discharge curve as the open circuit voltage as a function of the SoC (see Fig.7).

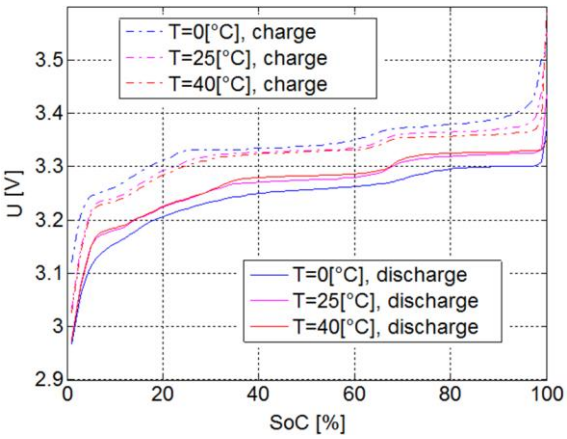

Figure6: Charge and discharge curve at T=0[°C], T=25[°C], and T=40[°C] at a charge and discharge rate of C/50.

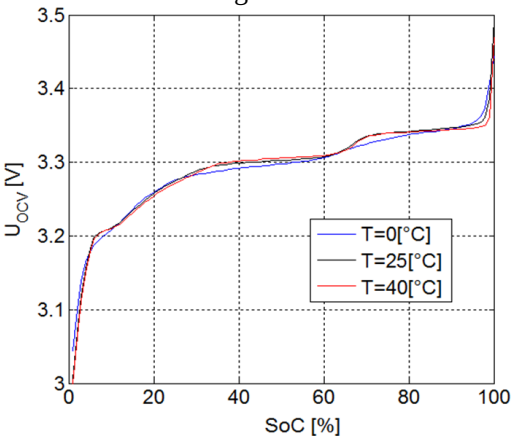

Figure7: Average terminal voltage of charge and discharge curve as a function of the SoC.

4.2.2 EIS-plot measurements

We measured the cell impedance as a function of the SoC at a temperature of 0 [°C], 25 [°C] and [40°C]. The measurements were carried out by means of an IVIUM STAT impedance analyzer in a frequency range of 50 [mHz] to 8 [kHz] while discharging the cell at a current rate of C/10. Fig.8 shows the EIS-plots that are made out of the measurement results. We have limited the frequency range of the EIS-plots from 50 [mHz] to 659 [Hz], because at higher frequencies the self inductance of the cell was getting the dominant impedance and we did not include this in our model.

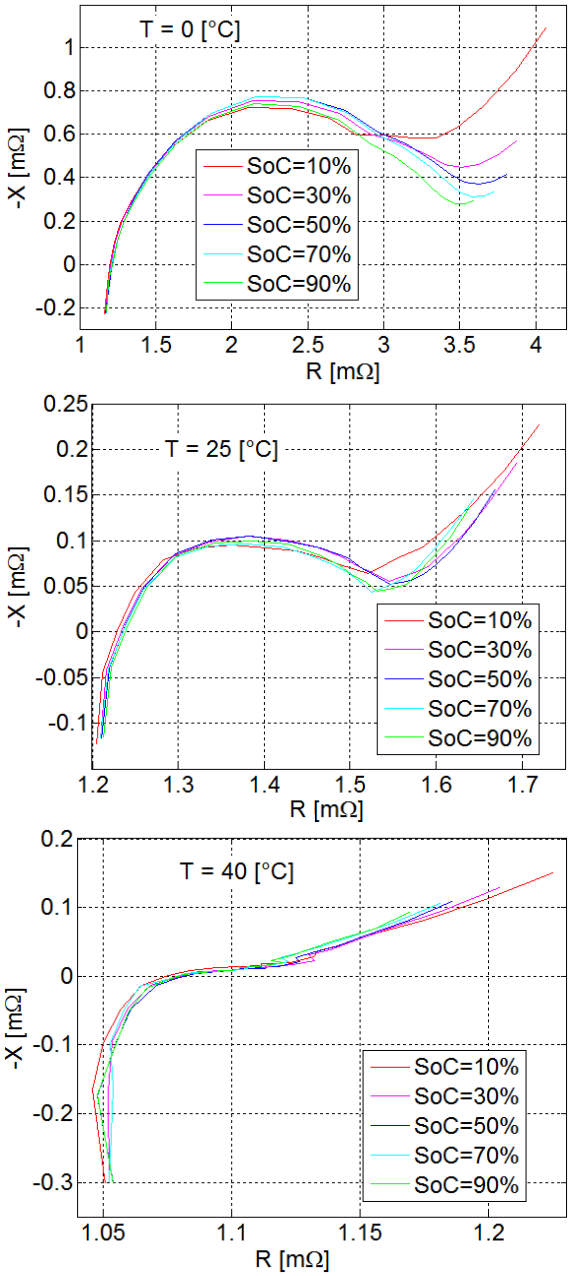

Figure8: EIS-plots of the cell impedance at three temperatures. The graphs show the impedances in the frequency range of 0.05[Hz] ≤f≤659 [Hz].

4.2.3 Current pulse measurement

We have measured the pulse response of 12 cells in series that are loaded by the pulse shaped current profile that is shown in Fig.9 and Fig 10. We have measured the pulse response for charge and discharge current pulses. The measurement has been performed at room temperature (22 [°C]).

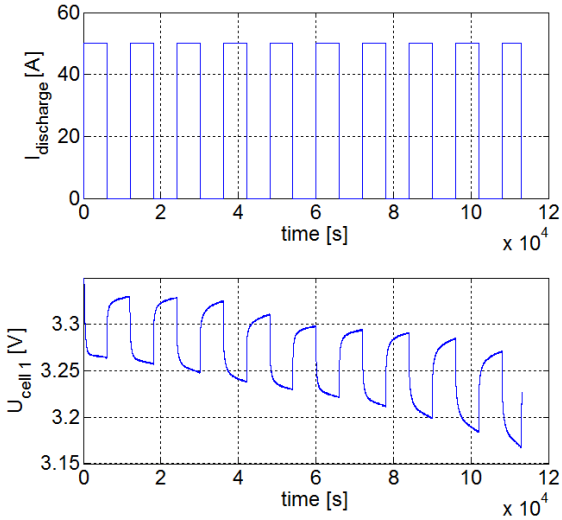

Figure9: Current and voltage of cell 1 during a discharge pulse current profile. Each pulse lasts 600 [s] and is followed by a 600 [s] rest period.

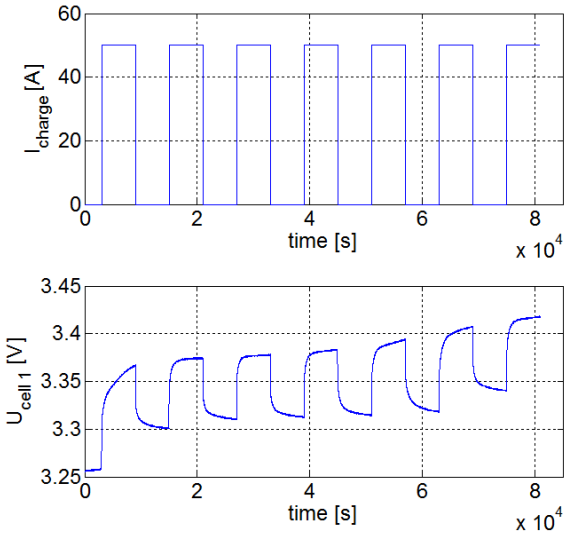

Figure10: Current and voltage of cell 1 during a charge pulse current profile. Each pulse lasts 600 [s] and is followed by a 600 [s] rest period.

4.2.4 Battery model

The base of our battery model is the practical circuit-based model proposed in [9]. This model reduces a typical Randell circuit that applies for LiFePO4 cells to a second order impedance circuit. We adapted this circuit to a third order circuit as shown in Fig.11. In Fig.11, R_b represents the bulk resistance, the parallel circuit of R_s and C_s models the activation polarization and the parallel circuits of $R_{la}//C_{la}$ and $R_{lb}//C_{lb}$ model the concentration polarization.

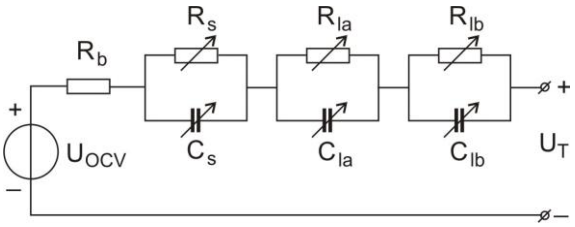

Figure11: Third order impedance circuit that is applied in our battery pack simulator.

We determined the values of C_s and R_s from the half circles of the EIS-plots. The EIS-plots of Fig.8 show that C_s and R_s have a hardly noticeable dependency on the SoC. Therefore, we neglected this dependency in our model. However, the EIS-plots of Fig.8 do show a dependency on the temperature. Table 2 shows the values of C_s and R_s that we found via curve fitting of the EIS-plots.

Table2: Values of R_s, C_s and τ_s at three temperatures. The time constant τ_s is calculated as: $\tau_s = R_s \cdot C_s$

T [°C]	R_s [mΩ]	C_s [F]	τ_s [ms]
0	1.4	6.4	9.0
25	0.24	21	5.0
40	0.04	88	3.5

We have investigated the dependency of R_s and C_s on charging and discharging at room temperature. We did not measure a clear dependency. Therefore, we assumed that the values above apply for both charging and discharging.

The values of R_{la}, R_{lb}, C_{la} and C_{lb} were determined from the pulse current measurements [10]. The sample time of the pulse current measurements was 0.1 [s]. This is more than 10 times higher than the time constant of the $R_s//C_s$ circuit, so the transient behavior of the measured pulse response is determined by the $R_{la}//C_{lb}$ and $R_{lb}//C_{lb}$ circuits.
By curve fitting of the cell voltage during the rest period intervals to equation 4, we found the values as a function of the state of charge.

$$U_{cell}(t) = U_0 + I_{puls} \cdot \left(R_{la} \cdot e^{\frac{-t}{\tau_a}} + R_{lb} \cdot e^{\frac{-t}{\tau_b}} \right) \quad (4)$$

Where: $U_{cell}(t)$ = cell voltage as function of time, U_0 = stationary voltage, I_{puls} = magnitude of current pulse (-50 [A] for discharge pulses and 50 [A] for charge pulses), $\tau_{la} = R_{la} \cdot C_{la}$ = time constant of the $R_{la}//C_{la}$ circuit, $\tau_{lb} = R_{lb} \cdot C_{lb}$ = time constant of the $R_{lb}//C_{lb}$ circuit.

We didn't measure the temperature dependency of R_{la}, R_{lb}, C_{la} and C_{lb}. Instead, we assumed that the temperature dependency of the concentration polarization of our cells is the same as is measured in [9] for $LiFePO_4$ cells. We used the empirical relations described in [9] and scaled them as follows:

Charging:

$$R_{lac}(soc,T) = R_{lac}(soc,22°C) \cdot \frac{R_{lc}(soc,T)}{R_{lc}(soc,22°C)}$$

$$R_{lbc}(soc,T) = R_{lbc}(soc,22°C) \cdot \frac{R_{lc}(soc,T)}{R_{lc}(soc,22°C)}$$

$$C_{lac}(soc,T) = C_{lac}(soc,22°C) \cdot \frac{C_{lc}(soc,T)}{C_{lc}(soc,22°C)}$$

$$C_{lbc}(soc,T) = R_{lbc}(soc,22°C) \cdot \frac{C_{lc}(soc,T)}{C_{lc}(soc,22°C)}$$

Discharging:

$$R_{lad}(soc,T) = R_{lad}(soc,22°C) \cdot \frac{R_{ld}(soc,T)}{R_{ld}(soc,22°C)}$$

$$R_{lbd}(soc,T) = R_{lbd}(soc,22°C) \cdot \frac{R_{ld}(soc,T)}{R_{ld}(soc,22°C)}$$

$$C_{lad}(soc,T) = C_{lad}(soc,22°C) \cdot \frac{C_{ld}(soc,T)}{C_{ld}(soc,22°C)}$$

$$C_{lbd}(soc,T) = R_{lbd}(soc,22°C) \cdot \frac{C_{ld}(soc,T)}{C_{ld}(soc,22°C)}$$

Where: $R_{lc}(soc,T)$, $R_{ld}(soc,T)$, $C_{lc}(soc,T)$ and $C_{ld}(soc,T)$ are the circuit parameter equations given in [9]. In the equations above, the subscript c is used for charging and d for discharging.

Fig.12 shows the values of R_{la}, R_{lb}, C_{la} and C_{lb} for charging and discharging.

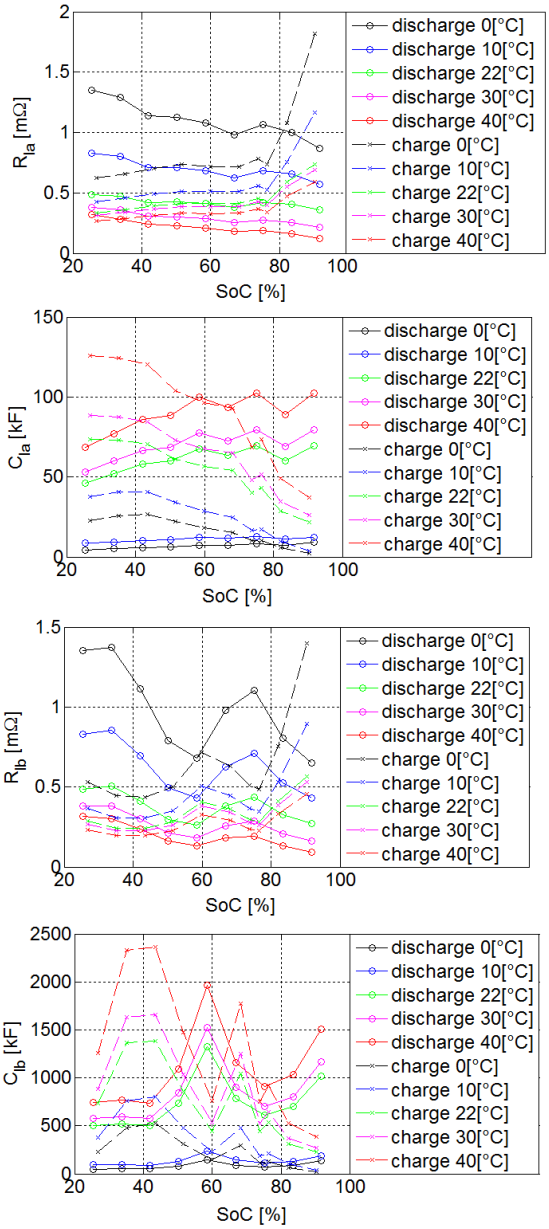

Figure12: Values of R_{la}, R_{lb}, C_{la} and C_{lb} for charging and discharging. The solid lines are the graphs for discharging; the dashed lines are the graphs for charging.

The bulk resistor R_b is determined from the pulse current measurements. Because the sample time is much larger than the time constant of the R_s//C_s and much smaller than the time constants of the R_{la}//C_{la} and R_{lb}//C_{lb} circuits, it applies:

$$R_b + R_s = -\frac{\Delta U}{\Delta I}$$

Where: ΔU and ΔI are the voltage and current change, measured at the end of the pulse and start of the rest period.

At T=22 [°C] we found for the sum of R_b and R_s: $R_b + R_s = 0.8$ [mΩ]. For the bulk-resistance we then find:

$R_b = 0.5$ [mΩ]

The value of R_b found above is about 0.6 [mΩ] less than the value that can be derived from the EIS-plots. This difference is caused by the contact resistance of the connections to the IVIUM STAT impedance analyzer that is used to measure the EIS-curves.

Finally, the SoC in our model is calculated by:

$$SoC = SOC_i - \frac{\int_0^t I \cdot dt}{C_i}$$

Where: SoC_i is the initial state of charge of cell i and C_i is the capacity of cell i.

5 Model validation

In this section we discuss the model validation. We do this by comparing the cell voltages and temperatures of the battery pack shown in Fig.4 to the simulated results of a model of the same pack. As the validation current profile, we used the measured current of the motor controller of an electric Fiat Doblo while driving the low power NEDC [11]. We have loaded the battery pack twice with the measured current. We introduced a 300 [s] rest period at the end of the first and second current profile. Fig.13 shows the validation current. The validation current varies between -203 [A] and 367 [A] and has a standard deviation of 94 [A]. The sample time of the validation measurement is 0.1 [s].

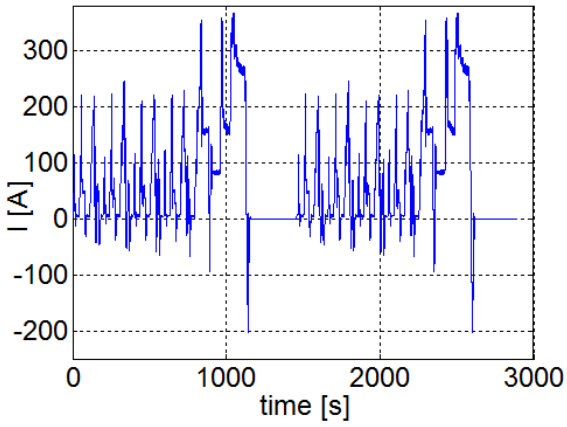

Figure13: Validation current profile

The measurement started with a fully charged battery pack at 21 [°C]. At the end of the measurement, the SoC was reduced to 49%.
Fig.14 shows the averaged measured and simulated cell voltage as a function of the time. We averaged the cell voltages of all cells. Fig.15 shows the difference of the averaged measured and simulated cell voltages.

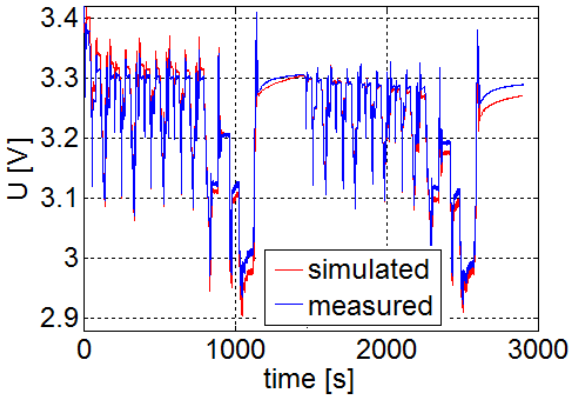

Figure14: Simulated and measured cell voltage. The simulated and measured voltages are averaged over all 12 cells.

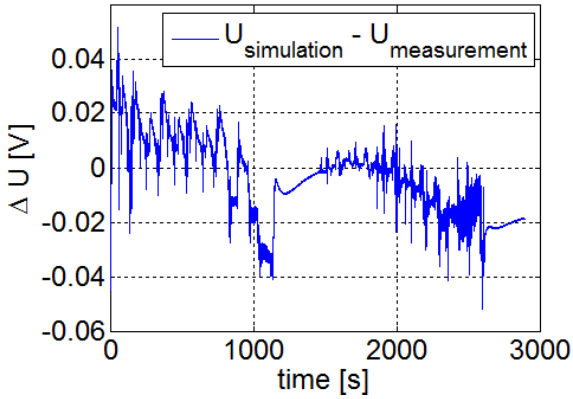

Figure15: Difference of the averaged simulated and measured cell voltage.

Fig.15 shows a gradual decreasing difference between the simulated and measured cell voltage of +20 [mV] at the start of the test to -20 [mV] at the end of the test. This might be explained by the hysteresis effect that is not taken into account by our model. Also the modeling of the activation polarization effects by only two parallel circuits of R and C might explain this difference.
The absolute difference of the simulated and measured voltages is in the entire time range below the 50 [mV]. The standard deviation of the difference of simulated and measured voltage is 14 [mV]. This can be translated to a difference in the overall resistance of 0.15[mΩ], which is about 10% of the sum of all resistances in the model.

Fig.16 shows the measured and simulated temperature of one cell at the edge of the pack and a cell in the middle of the pack. Also, the measured ambient temperature is shown.

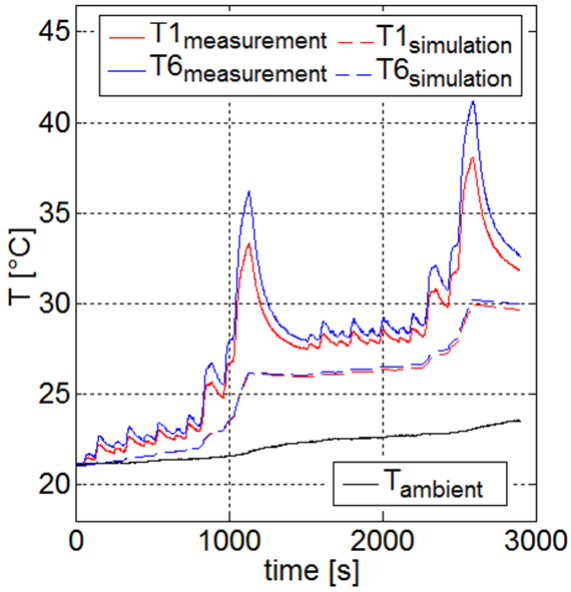

Figure16: Simulated and measured temperature of cell 1 at the edge of the battery pack and cell 6 in the middle of the battery pack. The black line is the measured ambient temperature.

Fig.16 shows that the difference between the simulated and measured temperatures gradually increases to about 2 [°C] at the end of the test. This difference can be explained by the raise of the ambient temperature during the measurement, while the ambient temperature in the model has been constant.
We also observe more high frequency components in the response of the measurements. We explain this by the heat dissipation at the poles caused by the contact resistance. The temperature sensors are mounted on the poles of the cells, so the measured temperatures are relatively strongly influenced by the local heat dissipation on and around the poles. In the model, the poles and connection strips are part of the heat capacity of the cell. No temperature gradients exist in the cell model which results in a flatter temperature graph.

6 Battery pack simulator tests

In order to evaluate the BPS, we have connected it to an Elithion Lithiumate Pro BMS. The BPS was loaded with the twelve cells battery pack model that is discussed in the previous sections. We tested the following features:

- The accuracy of the emulated cell voltages of the BPS compared to the model output.
- The transient behaviour of the emulated voltages.
- The SoC estimation of the BMS when it is connected to the BPS.
- The correct working of the under and over voltage detection of the BMS.
- The maximum sample rate of the BPS

As explained before, we cannot test the balancing functionality of the BMS because of the limited output current of the isolation amplifiers. Also, we did not connect the temperature sensors of the cell monitoring units of the BMS to our BPS, so the temperature related functionality of the BMS is not tested.

6.1 Accuracy of emulated voltages

The accuracy of the emulated voltages of the BPS is determined by comparing the measured emulated cell voltages to the model output. We use the current profile shown in Fig.13 for this test. The sample time of the test is 0.1 [s]. Fig.17 shows the emulated and simulated cell voltage of cell 1. The measured and simulated cell voltages of the other cells are comparable. The difference between both signals becomes only visible when zoomed in to a small area of the graph.

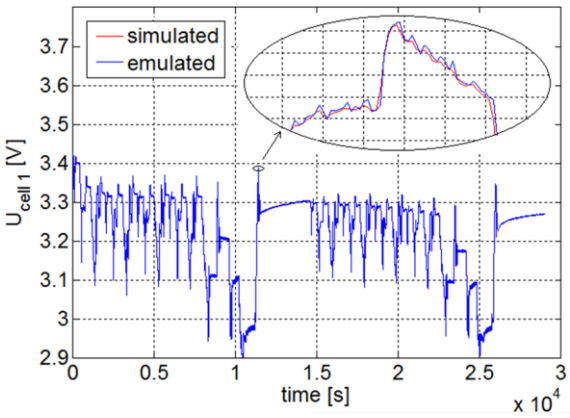

Figure17: Emulated and simulated voltage of cell 1 when the battery pack is loaded with the validation current profile of Fig13.

The standard deviation of the difference of the emulated and simulated signal is 1.1 [mV]. This corresponds to the resolution of the digital to analog converter that is used in the isolation amplifier circuit.

6.2 Transient behaviour of emulated voltages

We determined the transient behaviour of the isolation amplifiers by measuring the rise and fall time on a step response. For this test, we emulated a current sensor with a sensitivity of 100 [A/V]. We examined the current sensor output voltage on an oscilloscope when a block shaped current is simulated that alternates between -200 [A] and +200 [A] at a frequency of 10 [Hz]. Fig.18 shows the rising and falling edge of the emulated current sensor voltage.

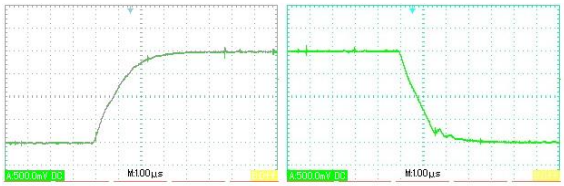

Figure18: step response of the isolation amplifier on the rising edge (left scope image) and falling edge (right scope image) of a block shaped pulse. The time scale of the scope images is 1 [µs/div].

Fig.18 shows a rise time of about 3 [µs] and a fall time of 2 [µs]. This is much less than the minimum simulation time of 254 [µs] that originates from the limitations of the SPI bus. This means that the transient behaviour of the hardware hardly plays any role in the dynamic behaviour of the whole system.

6.3 Evaluation of SoC determination

We evaluated the SoC determination of BMS by simulating the battery pack when it is loaded by a current profile that consists of twice the validation current profile shown in Fig.13. Figure 19 shows the SoC, simulated by the BPS, and the SoC estimation of the BMS as a function of the time.

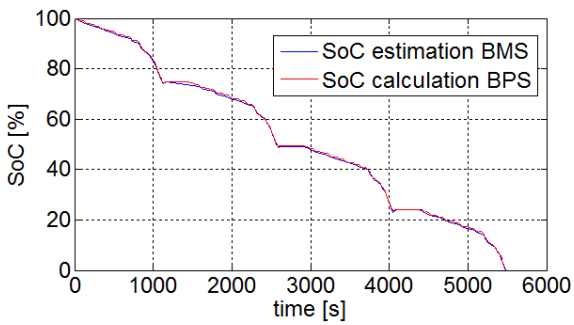

Figure 19: SoC estimation of the BMS and the SoC calculated by the model.

The difference between the SoC estimation of the BMS and the SoC calculation of the model is less than 0.5%. This corresponds to the resolution of the SoC estimation of the BMS, which is 1%.
We also tested the response of the SoC estimation by the BMS on a stepwise change of the SoC of the BPS from 10% to 90%. We saw that the SoC of the BMS estimation did not change. Instead, we saw that the state of health (SoH) was adapted by this change. We also entered a stepwise change of the SoC when the BMS was switched off. Again, the BMS did not report a change in the SoC estimation after turning it on again.
It seemed to us that the SoC estimation was only readapted to 100% after the maximum cell voltage was reached while charging the battery.

6.4 Under and overvoltage detection

Under and overvoltage detection is tested by changing the SoC of the BPS abruptly so that the cell voltages exceeded the under and overvoltage limits. We found that the BMS detected the exceeding of the limits correctly.

6.5 Maximum sample rate

The data transfer on the SPI bus sets the upper limit of the sample rate to 3.9 [kSamples/s]. This limit however may be decreased by the execution time of the model. The execution time depends heavily on the speed performance of the xPC target, the complexity of the model and the number of cells of the battery pack. Table 3 lists the execution time of the model that is described in this paper as a function of the number of cells. We have used a common PC with pentium 4 3.00 GHZ processor and 4 GByte RAM as xPC target.

Table3: Execution time of the model as a function of the number of cells.

number of cells	1	2	3	6	12
execution time [µs]	13.9	16.1	17.5	21.6	30.2
number of cells	24	48	60	120	248
execution time [µs]	48	84	103	207	477

For our model and xPC target, it applies that the maximum sample rate decreases below 3.9 [kSample/s] when the number of cells is more than 140.

For most battery management systems, this sample rate is sufficiently high and there is enough space to implement more complex models that take more calculation time.

7 Conclusions and further study

The BPS, proposed in this abstract, provides a flexible architecture that can be used to emulate cell voltages and temperatures of a battery pack. We evaluated the BPS by implementing a $LiFePO_4$ battery pack. Test results show that relatively complex models can be simulated at high sample-rates with an acceptable accuracy.
We connected a Lithiumate Pro BMS to our BPS. We found that the basic functionality of this BMS could be tested well with our BPS.
A major shortcoming of the BPS now is the lacking of the capability to test the balancing feature of BMS. Further work will focus on the implementation of this.

Acknowledgments

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